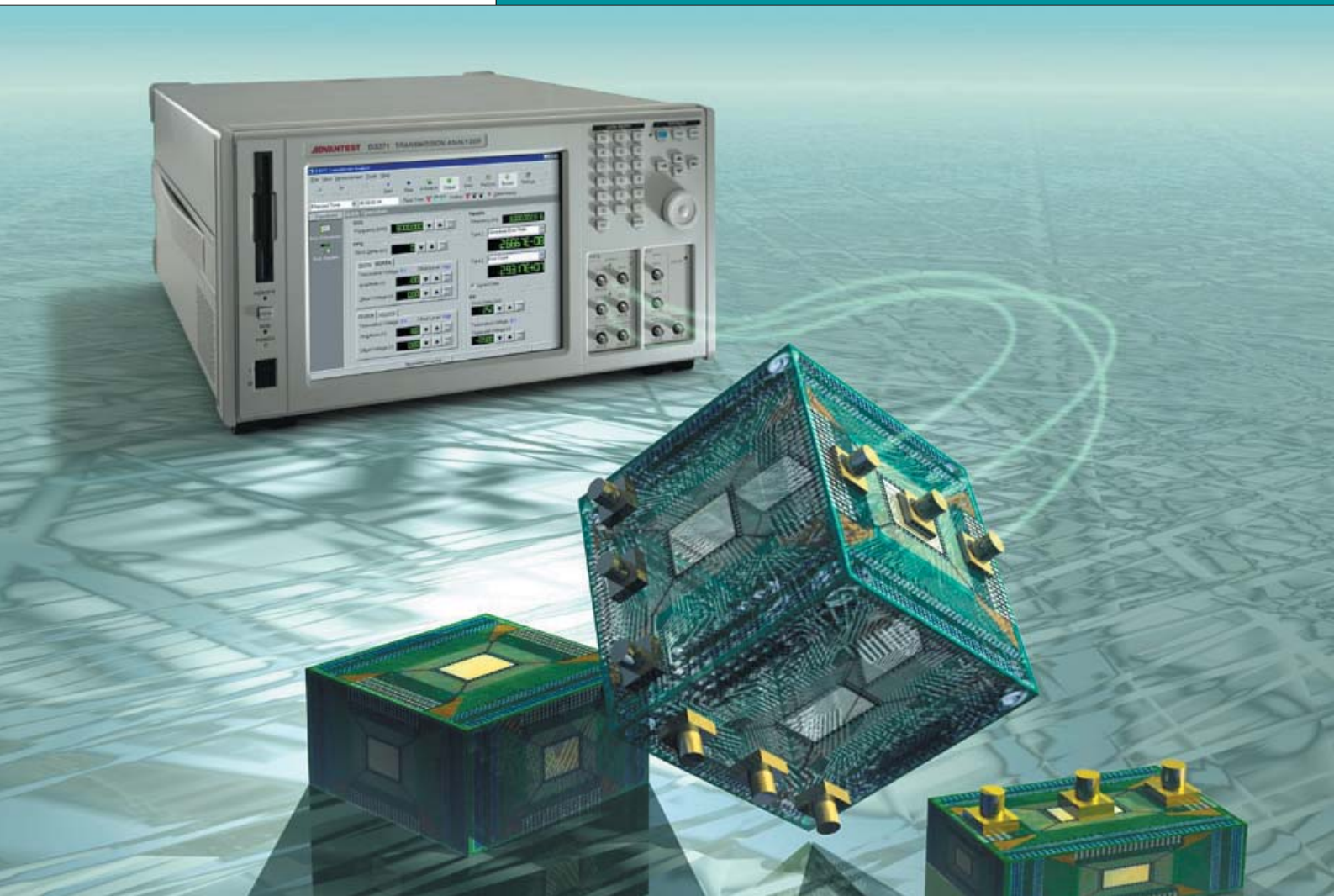
ADVANTEST

D3371
3.6 GHz Transmission Analyzer

Compact Integration of a Pulse Pattern Generator and Bit Error Detector.

Wide Variety of Measurement Options for Gigabit Ethernet and SONET/SDH.

D3371



The volume of communications data on the Internet has been growing very quickly. This has caused a continuing rapid expansion of capacity in backbone networks and computer networks.

The D3371 Transmission Analyzer has a variable data rate capability from 10 MHz to 3.6 GHz which encompasses all data rates necessary for SONET/SDH, Fiber Channel, and Gigabit Ethernet devices required for the IP network markets. It can also generate various types of PRBS and user programmable test patterns for simulating actual line traffic, enabling flexible accommodation of a wide range of needs from development to production and ongoing maintenance.

- **Excellent output waveform quality**
- **3 Vp-p maximum, wide range of output amplitudes from low-amplitude devices to direct Laser Diode modulation and Electro Absorption modulators**
- **Capability to generate diverse test patterns for Gigabit Ethernet and SONET/SDH**
  - Pseudo random (PRBS) pattern
  - Programmable pattern
  - Zero substitution pattern
  - STM (SONET/SDH) frame pattern
  - Flexible pattern
- **Significantly enhanced bit error measurement functions**
  - Error rate measurement
  - Error count measurement
  - Error interval measurement
  - Error-free interval measurement
  - Frequency measurement
  - Error performance measurement
- **Burst pattern signal generation capability**
- **High-precision 10 MHz to 3.6 GHz internal synthesized clock generator**
- **Auto search function**
- **GPIB Remote control function**
- **10Base-T Ethernet interface**
- **Interactive GUI with large color LCD, touch panel**

Windows® application software

Free, non-warranted software provides these capabilities.

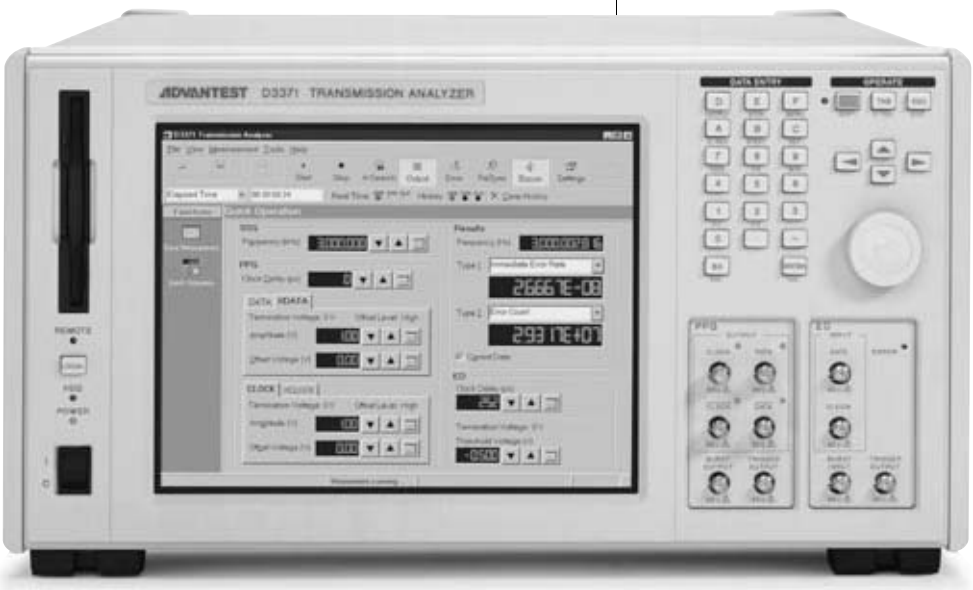
- 8B/10B code editor software for Gigabit Ethernet pattern creation
- Pattern editor/converter software enabling easy data creation
- Q-FACTOR measurement, Eye margin measurement, and BER (Bit Error Rate) diagrams measurement software

Module options

- OPTION 10: Pulse Pattern Generator (2 Vp-p output) module
- OPTION 11: Pulse Pattern Generator (3 Vp-p output) module
- OPTION 12: Error Detector module
- OPTION 13: 3.6 GHz synthesizer module

Measurement function options

- OPTION 70: Jitter Tolerance option
- OPTION 71: Pattern option
- OPTION 72: Error phase analysis option



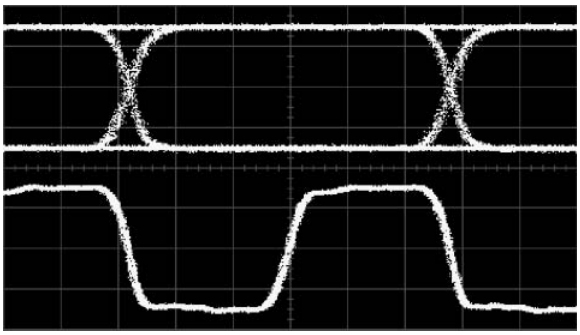
Pulse Pattern Generation Module
(OPTION 10: 2 Vp-p output)
(OPTION 11: 3 Vp-p output)

Pulse Pattern Generation Function

Optimum for evaluating devices and module characteristics

High-quality data patterns can be generated for evaluating the characteristics of optical devices (requires user supplied E/O and O/E optical interfaces) and sub-systems for data communications. It is possible to generate a maximum of 8 M-bits of user programmable patterns, PRBS patterns (2^7-1 to 2^{31}-1, with adjustable Mark/Space ratio), and user settable zero substitution patterns. It is also easy to vary the amplitude, offset and cross point for the output data and clock waveform.

3.6 GHz, 1 Vp-p, 0 V offset



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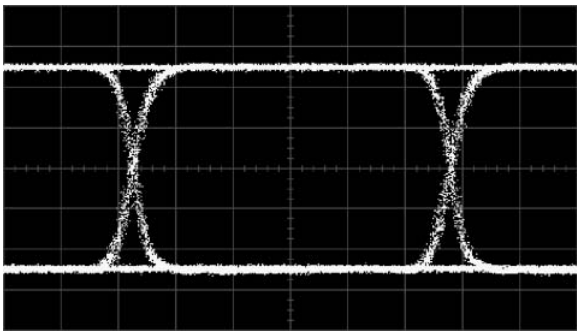
Output waveform of data and clock

3.6 GHz, 2 Vp-p, 0 V offset



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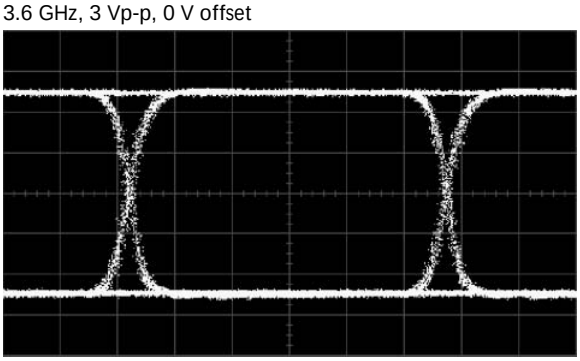
Output waveform of data

The Pulse Pattern Generator has a wide output range suitable for evaluation of Electro Absorption modulators and Laser Diodes

It is easy to output patterns to suite various types of devices from low-amplitude devices to high-level input EA modulators. (max. 3 Vp-p output: OPTION 11)

3.6 GHz, 3 Vp-p, 0 V offset



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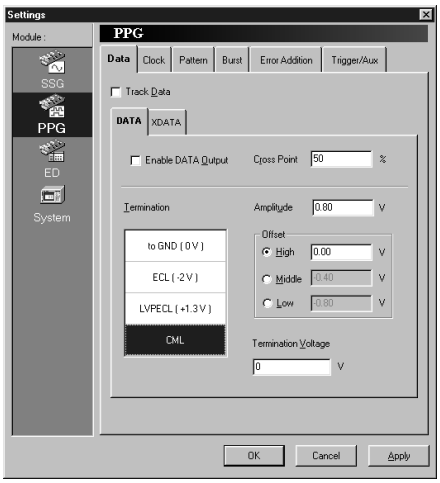
Output waveform of data

Easy Set Up for Pulse Pattern Generator

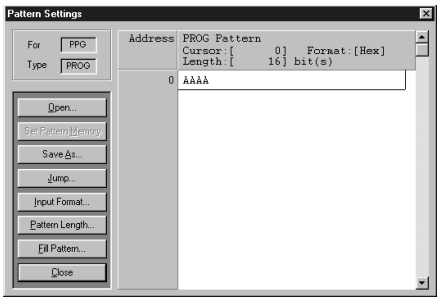
The pattern generator section settings can be changed or verified with ease using the common MS Windows and touch screen interface. Burst data can also be easily output.
The interface is also applicable to ECL/LVPECL/CML and GND termination.



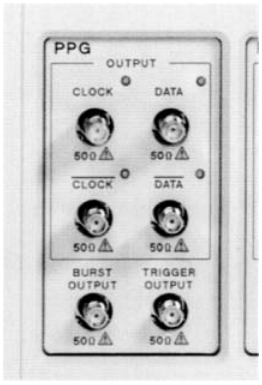
Example setting of Pulse Pattern Generator

Easy Creation of Programmable Patterns

Using the internal pattern editor enables to easily construct, store and recall data patterns up to approximately 8 M-bits in length. It is also possible to store and recall a pattern created on an external personal computer via GPIB or floppy disk.



Example display of Programmable Pattern editor



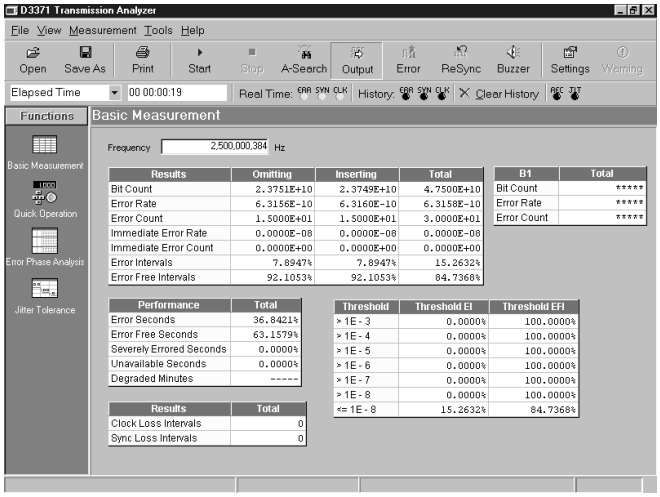
Pulse Pattern output connector

Error Detector Module (OPTION 12)

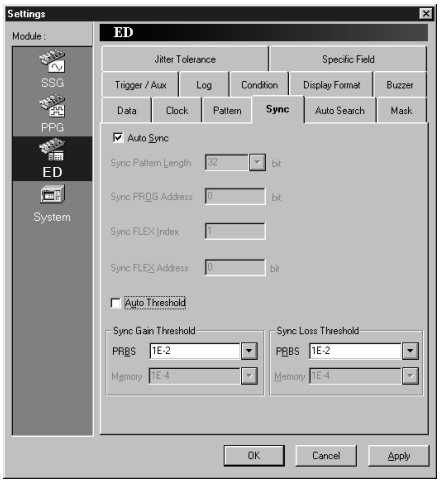
Bit Error Measurement Function

Automatic Setting of Optimum Measurement Values using the Auto Search Function

The Auto Search Function allows for automatically setting the PRBS pattern, input data threshold voltage and input clock phase to values optimum for measurement. It is also possible to conduct measurements on a test system with a large error rate (about 10^{-2}) by optionally setting the synchronization determination threshold value. In addition, combining the Error Detector module with the Pulse Pattern Generator module enables bit error measurement using burst data, allowing easy execution of a loop-back test with optical fiber cable. It is also possible to save the measurement result logs in text file form.



Example display of Basic Measurement result



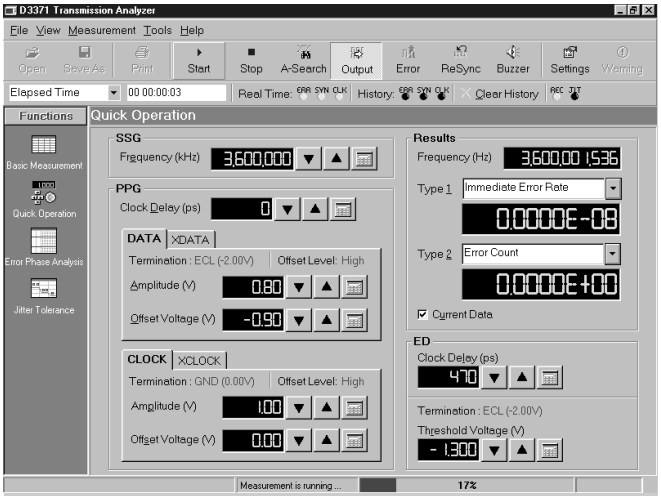
Setting display of synchronization threshold

Masked Data Measurement

By specifying the measurement start bit and measurement stop bit, it is possible to measure the bit error rate of only specific bits of the data received by the error detector. In addition, with the pattern option (OPTION 71), it is also possible to measure the bit error rate of specific bits of the STM (SONET/SDH) frame or flexible patterns.

Easy Setting of Basic Measurement Conditions in the Quick Operation Window

The Quick Operation window is provided so that the user can easily set up and execute the basic measurement conditions. The frequently varied measurement condition settings and the measurement results can be visually confirmed enabling easy operation.



Example display of Quick Operation

3.6 GHz Synthesizer Module (OPTION 13)

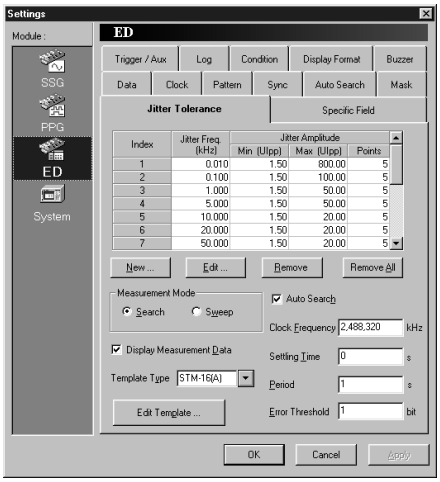
The synthesizer module (10 MHz to 3.6 GHz) can be installed to provide an internal high-frequency resolution, high accuracy, and reduced SSB phase noise clock source.

Setting display of synthesizer module

Jitter Tolerance Option (OPTION 70)

Jitter Tolerance Measurement Function

By setting the jitter frequency to be added, jitter amplitude value (minimum value and maximum value), and the number of measurement points with respect to the specified clock frequency, jitter tolerance measurements can be performed. However, it is necessary to use the Pulse Pattern Generator module (OPTION 10/11), Error Detector module (OPTION 12), and 3.6 GHz Synthesizer module (OPTION 13).



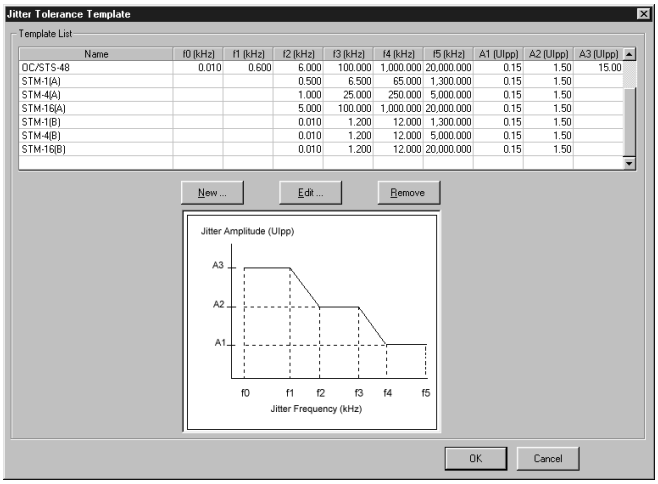
Setting display of jitter tolerance measurement

Measurement Using User-Defined Templates

OC/STS-1, 3, 12, and 48 * and STM-1, 4 and 16 ** can be selected as a default template for jitter tolerance measurement. Measurement using user-defined templates is also possible.

**: Reference standards: Bellcore GR-253-CORE*

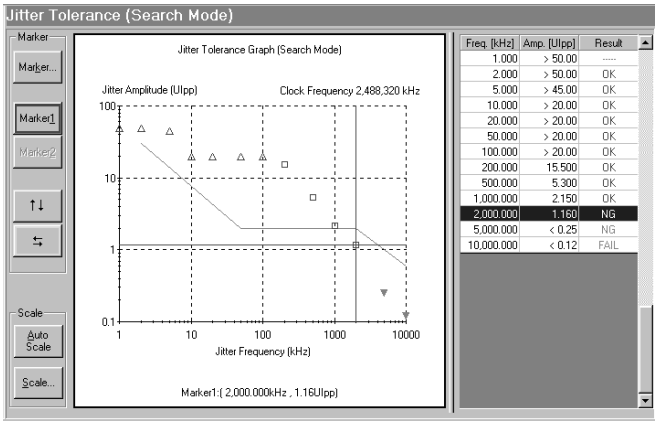
***: Reference standards: ITU-T G.958*



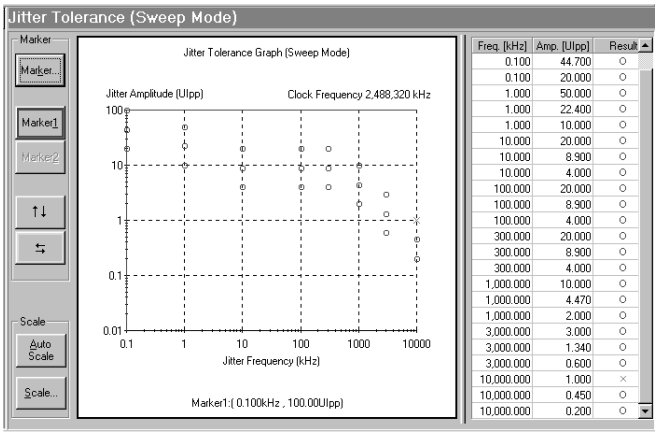
Example display of template

Graphical Display of Automatic Measurement of Jitter Tolerance

The jitter tolerance is measured automatically by setting the jitter tolerance measurement condition. The result is displayed using a graph and table.
In addition, automatic pass/fail and display is possible by setting the error threshold (bit error value) for pass/fail determination. In the Search mode, the jitter tolerance point is automatically detected from measurement points specified for each jitter frequency and displayed.
In the sweep mode, the software judges whether the value is equal to or smaller than the error threshold (bit error value) or not (pass or fail) at all the specified measurement points.



Example display of Search Mode Measurement

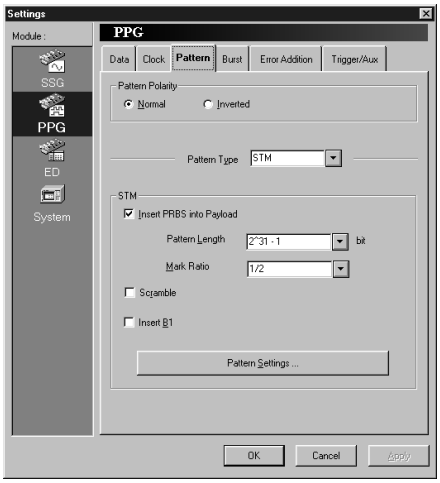


Example display of Sweep Mode Measurement

Pattern Option (OPTION 71)

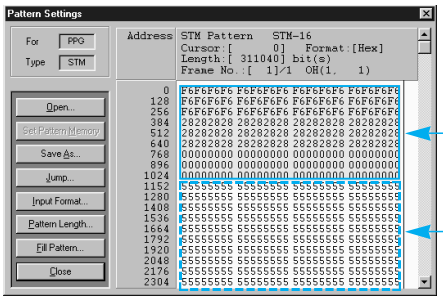
STM (SONET/SDH), Flexible Pattern Function

There are two different Pattern options: STM (SONET/SDH) pattern and FLEX pattern. Pattern options are used together with the Pulse Pattern Generator module (OPTION 10/11) and Error Detector module (OPTION 12).
In the STM (SONET/SDH) pattern, it is possible to easily create data with the frame structure conforming to ITU-T G.707 recommended. For the overhead area, any data pattern created by the programmable pattern creation function can be used. For the payload area, a programmable pattern or PRBS pattern can be selected. In addition, it is possible to set B1 insertion and scramble addition conforming to ITU-T G.707 recommended.
Overhead error, payload error, and B1 error measurement can also be performed.



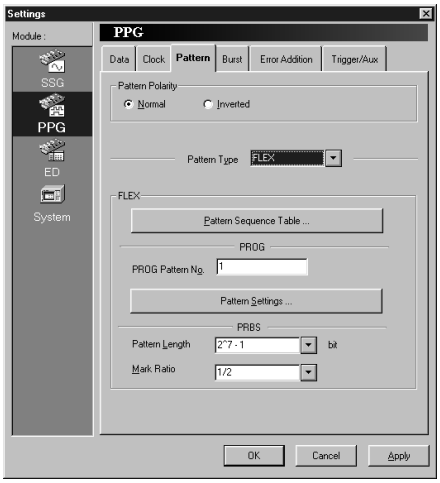
Example display of STM (SONET/SDH) pattern setting

The STM (SONET/SDH) pattern creation screen allows creation of the overhead area and payload area.

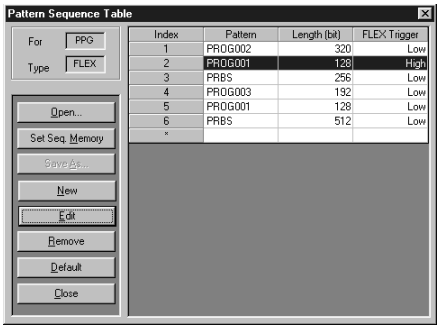


Example display of STM (SONET/SDH) pattern creating

It is possible to create a FLEX pattern through the combination of the Programmable pattern and PRBS pattern. The combination, generation order, and generation bit length can be defined in the pattern sequence table.
This function makes it possible to easily create an IP header and IP data with the PRBS pattern used in the data section. By using the error phase analysis function (OPTION 72), it is possible to locate the errored bit position of the IP data.



Example display of FLEX pattern setting



Example display of FLEX pattern creating

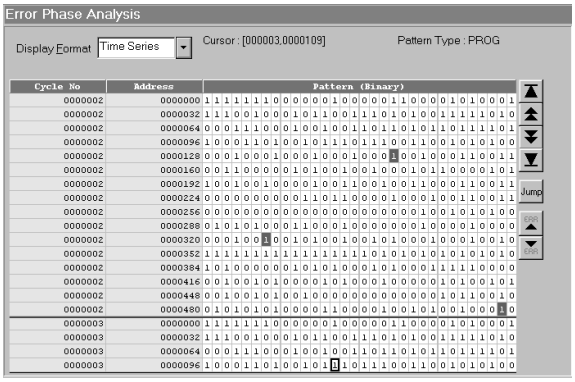
Error Phase Analysis Option (OPTION 72)

Error Phase Analysis Function

Error phase analysis is used together with the Error Detector module (OPTION 12). It is performed at the same time as the bit error measurement to continuously record bit error positions. By analyzing the errored bit position information after completion of a bit error measurement, the causes of the bit error(s) may be more easily determined.
In addition, errored bits in a specific area can also be recorded. The result of an error phase analysis can be displayed in time sequence or statistical form.

Displaying Result in Time Sequence

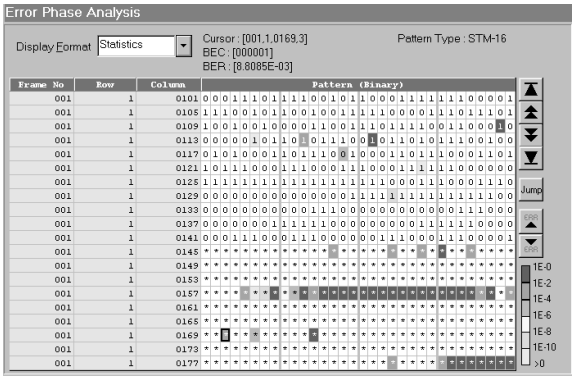
The pattern information and error bit position are displayed in time sequence. The PRBS pattern contained in the STM (SONET/SDH) pattern or FLEX pattern can also be displayed. Usable patterns include the programmable pattern, Zero Substitution pattern, STM (SONET/SDH) pattern and FLEX pattern. The PRBS pattern cannot be used separately.



Example display of Error phase analysis (Time Sequence display)

Displaying the Result in Statistical Form

The statistics data display includes the number of bit errors and bit rate for each bit of the pattern. Error bits are displayed in different colors for each bit error rate.

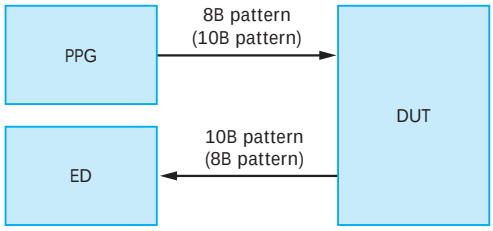


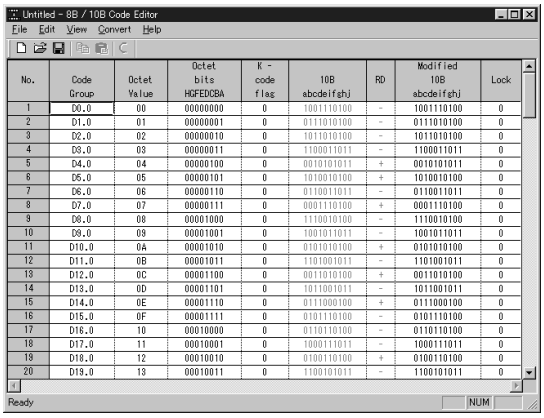
Example display of Error phase analysis (Statistics Display)

Wide Variety of Windows Application Software

8B/10B code Editing Function for Gigabit Ethernet

By using the 8B/10B code editor function, user-defined 8 bit patterns can be converted to 10 bit patterns automatically. Since the created 8 bit pattern and 10 bit pattern can be used with the pulse pattern generation function, the 10 bit pattern can easily be transferred to devices, modules, and communication equipment for Gigabit Ethernet. In addition, the 8 bit pattern and 10 bit pattern can also be used with the error detector function.

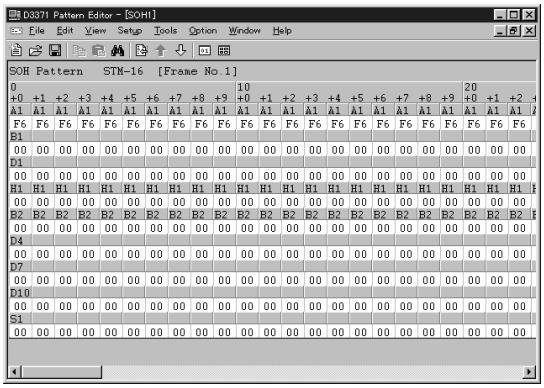




Example display of 8B/10B code editor function

Pattern Editor Function

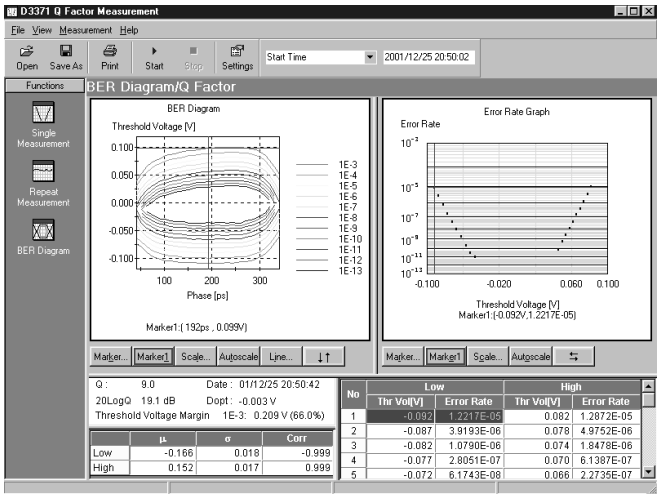
Although any patterns can be created and edited directly on the D3371, the use of the external pattern editor software makes it easier to create and edit patterns on a PC.



Example display of pattern editor function

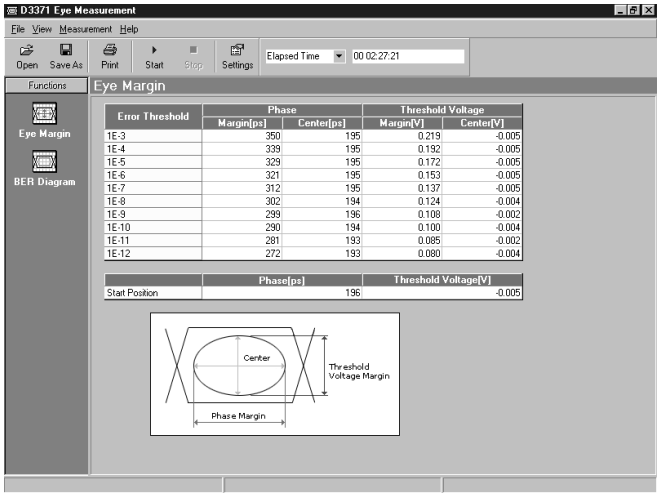
Q-FACTOR Measurement, Eye Margin Measurement, and BER Diagrams Measurement Functions

Using a GPIB connection to a Windows-based PC to control the D3371, Q-FACTOR measurement, Eye margin measurement, and BER diagrams measurement can be performed. In a Q-FACTOR measurement, the "threshold voltage vs. bit error rate" can be displayed.



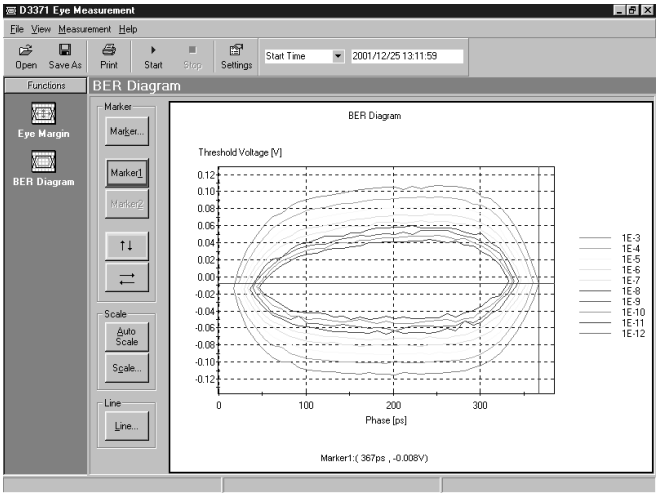
Example display of Q-FACTOR measurement result

In the Eye margin measurement, the phase margin and threshold voltage margin are measured while varying the phase and threshold voltage so that the specified error rate is not exceeded.



Example display of Eye margin measurement result

In a BER diagram measurement, points of the specified error rate are connected and displayed while varying the threshold voltage and phase. As an application of Q-FACTOR measurement, it is also possible to perform BER diagrams measurement by measuring the error rate for a short time.



Example display of BER diagrams measurement result

Specifications

D3371 Main Unit

System Function

OS:	Microsoft® Windows 98 Second Edition
Main memory:	128 MB
Display unit:	10.4 inch TFT LCD color display with the touch panel functions 800 x 600 pixels, with a back-light
Floppy disk drive:	3.5 inches in two modes (720 KB/1.44 MB)
Hard disk:	3.5 inches (6 GB or more)
Operating part:	Panel keys and the touch panel
Remote control:	GPIB compliant with IEEE 488.2
Measurement time base accuracy:	±10 ppm

Input/Output

Parallel connector:	D-sub25 pins
USB connector:	Type A connector, 2 channels installed for the keyboard and mouse
Ethernet connector:	10 Base-T
GPIB Connector:	IEEE 488.2 bus connector

General Descriptions

Operating environment range:	+5 to +40°C Relative humidity; 40 to 85% (without condensation)
Storage environment range:	-20 to +70°C Relative humidity; 30 to 85% (without condensation)
AC input power source:	100 VAC and 200 VAC systems are switched automatically 100 VAC system operation; 100 to 120 V, 50/60 Hz 200 VAC system operation; 220 to 240 V, 50/60 Hz
Power consumption:	160 VA or below
Mass:	21 kg (46.3 lbs.) or less (module, accessories, and so on are not included)
Dimension:	Approximately 424 (W) x 221 (H) x 500 (D) mm (approximately 16.7 (W) x 8.7 (H) x 19.7 (D) in.) (the protrusions of the rear feet, connectors, and so on are not included)

2 Vp-p or 3 Vp-p Output Module of the Pulse Pattern Generator (PPG Module)
(2 Vp-p Output: OPTION 10, 3 Vp-p Output: OPTION 11, Pattern: OPTION 71)

Generated Pattern

Pseudo random (PRBS) pattern

Pattern length: $2^n - 1$ (n: 7, 9, 10, 11, 15, 23, 31)

Number of stages and generating function:

Number of stages	Generating function	Standard
7	$X^7 + X^6 + 1$	ITU-T recommended V. 29
9	$X^9 + X^5 + 1$	ITU-T recommended V. 52
10	$X^{10} + X^7 + 1$	
11	$X^{11} + X^9 + 1$	ITU-T recommended O. 152
15	$X^{15} + X^{14} + 1$	ITU-T recommended O. 151 (1/2)
23	$X^{23} + X^{18} + 1$	ITU-T recommended O. 151 (1/2)
31	$X^{31} + X^{28} + 1$	

Mark ratio (variable): 1/2, 1/4, 1/8, 0/8, $\overline{1/2}$, 3/4, 7/8, 8/8

Mark ratio and number of bit shift: 1 bit

Programmable (PROG) pattern

Pattern length: 1 to 8,388,608 (2^{23}) bit

Pattern length and variable setting resolution [bit]:

Pattern length range	Setting resolution
1 to 262,144	1
262,146 to 524,288	2
524,292 to 1,048,576	4
1,048,584 to 2,097,152	8
2,097,168 to 4,194,304	16
4,194,336 to 8,388,608	32

Zero substitution (ZSUB) pattern

Pattern length: 2^n (n: 7, 9, 10, 11, 15) bit

Continuous zero bit length and setting resolution [bit]:

ZSUB pattern length	Continuous zero bit length range	Setting resolution
2^7	7 to 127	1
2^9	9 to 511	1
2^{10}	10 to 1023	1
2^{11}	11 to 2047	1
2^{15}	15 to 32767	1

STM (SONET/SDH) pattern (OPTION 71)

Frame structure:	STM-4, STM-16
Number of frames:	STM-4; 1 to 107 frames STM-16; 1 to 26 frames
Payload types:	Can be selected from PROG pattern and PRBS pattern
Scrambling:	Can be provided
B1 byte:	Can be provided

Flexible (FLEX) pattern (OPTION 71)

Number of patterns:	PROG pattern; 127 types PRBS pattern: 1 type
Pattern length:	PROG pattern; 128 to 65,536 bits (setting resolution: 64 bits) PRBS pattern; 128 to 2,097,152 bits (setting resolution: 64 bits)
Number of combined patterns:	1 to 1024 pattern(s)
Pattern logic:	Can be logically inverted

Error Addition

Mode:	Repeat, Single and External
Error addition route:	Route; 1 to 16

Burst

Mode:	Internal generation burst, External burst

Trigger

Mode:	Can be selected from the 1/8 clock, 1/32 clock, pattern phase, Frames (OPTION 71) and Flexible (OPTION 71)
Pattern phase:	PRBS Pattern; output position can be varied in increment of 1 bit PROG Pattern; output position can be varied in increment of 16 bit ZSUB Pattern; output position can be varied in increment of 16 bit
Frames (OPTION 71):	Output position can be set for each frame separately on a 16 bit basis
Flexible (OPTION 71):	The Low level or High level can be set for each pattern

AUX

Data types:	The Low level is output for PROG pattern The High level is output for PRBS pattern

Clock Input

Input amplitude:	0.5 to 2 Vp-p
Input waveform:	Rectangular wave or Sine wave (175 MHz to 3.6 GHz) Rectangular wave (10 to 175 MHz)
Duty ratio:	50 ± 5%
Input impedance:	50Ω (nominal) to 0 V
Connector:	SMA female

Data Output

Frequency:	10 MHz to 3.6 GHz
Number of output paths:	2 paths (each of DATA and $\overline{\text{DATA}}$)
Mode:	NRZ
Coupling:	DC
Amplitude range 2 Vp-p output module (OPTION 10) 3 Vp-p output module (OPTION 11):	To GND; 0.3 to 2 Vp-p setting resolution: 10 mV (OPTION 10) 0.3 to 3 Vp-p setting resolution: 10 mV (OPTION 11) ECL (to -2V); 0.6 to 1 Vp-p setting resolution: 10 mV LVPECL (to +1.3 V); 0.6 to 1 Vp-p setting resolution: 10 mV CML (to Vcc); 0.3 to 1 Vp-p setting resolution: 10 mV Exception; Vcc (termination voltage) is set between 0 and 3.5 V in 50 mV setting resolution
Offset range:	To GND; -2.0 to +2.0 V (High) setting resolution: 10 mV ECL (to -2 V); -1.0 to -0.6 V (High) setting resolution: 10 mV LVPECL (to +1.3 V); +2.3 to +2.7 V (High) setting resolution: 10 mV CML (to Vcc); Vcc -0.2 V to Vcc +0.2 V (High) setting resolution: 10 mV Exception; Vcc (termination voltage) is set between 0 V and 3.5 V in 50 mV setting resolution When the amplitude setting exceeds 2 Vp-p; -1.0 to +1.0 V (High) setting resolution: 10 mV (to 0 V)
Display:	Can be switched to High, Middle, Low
Rise and fall times:	60 ps (10 to 90%) or less (output amplitude ≥0.5 Vp-p) 80 ps (10 to 90%) or less (output amplitude <0.5 Vp-p)
DATA/$\overline{\text{DATA}}$ tracking function:	Yes. User selectable
Variable cross-point:	Yes. User selectable
Load impedance:	50Ω
Connector:	SMA female

Clock Output

Number of output paths:	2 paths (each of CLOCK and $\overline{\text{CLOCK}}$)
Coupling:	DC
Amplitude range:	To GND; 0.3 to 2 Vp-p setting resolution: 10 mV ECL (to -2 V); 0.6 to 1 Vp-p setting resolution: 10mV LVPECL (to +1.3 V); 0.6 to 1 Vp-p setting resolution: 10mV CML (to Vcc); 0.3 to 1 Vp-p setting resolution: 10mV Exception; Vcc (termination voltage) is set between 0 V and 3.5 V in 50 mV setting resolution
Offset range:	To GND; -2.0 to +2.0 V (High) setting resolution: 10mV ECL (to -2 V); -1.0 to -0.6 V (High) setting resolution: 10mV LVPECL (to +1.3 V); +2.3 to +2.7 V (High) setting resolution: 10mV CML (to Vcc); Vcc -0.2 V to Vcc +0.2 V (High) setting resolution: 10 mV Exception; Vcc (termination voltage) is set between 0 V and 3.5 V in 50 mV setting resolution
Display:	Can be switched to High, Middle, Low
Rise and fall times:	60 ps (10 to 90%) or less (output amplitude ≥0.5 Vp-p) 80 ps (10 to 90%) or less (output amplitude <0.5 Vp-p)
Clock delay:	±1 ns (setting resolution: 1 ps)
Load impedance:	50Ω
Connector:	SMA female

Burst Input

Input level:	0/-1 V
Input impedance:	50Ω (nominal) to 0 V
Connector:	SMA female

Burst Output

Output level:	0/-1 V
Load impedance:	50Ω to 0 V
Connector:	SMA female

Error Input

Input level:	0/-1 V
Input impedance:	50Ω (nominal) to 0 V
Connector:	SMA female

Trigger Output

Output level:	0/-1 V
Load impedance:	50Ω to 0 V
Connector:	SMA female

General Descriptions

Operating environment range:	+5 to +40°C Relative humidity; 40 to 85% (without condensation)
Storage environment range:	-20 to +70°C Relative humidity; 30 to 85% (without condensation)
Power consumption:	120 VA or below
Mass:	6.0 kg (13.2 lbs.) or less

Error Detector Module (ED Module: OPTION 12, Pattern: OPTION 71, Error Analysis: OPTION 72)

Measurement

Error rate:	0.0000 x 10^{-17} to 1.0000 x 10^{-0}
Error count:	0 to 4294967294 (Integer format) 0 to 9.9999 x 10^{16} (Exponent format)
Error interval (EI):	0 to 4294967294 (Integer format) 0.0000 to 100.0000% (Percentage format)
Error free interval (EFI):	0 to 4294967294 (Integer format) 0.0000 to 100.0000% (Percentage format)
Frequency measurement (input clock) accuracy:	10,000,000 to 3,600,000,000 Hz ±10 ppm ± 1 kHz
Error performance:	ES; Errored Seconds EFS; Error Free Seconds SES; Severely Errored Seconds US; Unavailable Seconds DM; Degraded Minutes
Threshold EI/EFI:	10^{-3} to 10^{-9}
B1 error (OPTION 71):	Available

Measurement Timer

Timer mode:	SINGLE, REPEAT, UNTIMED
Timer measurement period:	00 days 00 hours 00 minutes 01 seconds - 99 days 23 hours 59 minutes 59 seconds
Measurement interval timer:	0.1/1 s
Measurement time base:	±10 ppm (supplied by the D3371 main unit)

Error Analysis (OPTION 72)

Number of recording iterations:	1 to 131,071 point(s)
Result display format:	Time-series display (list format), statistics display (list format)

Automatic Search

Automatic search function:	Phase, threshold voltage, PRBS pattern

Synchronization

Synchronization threshold	
Mode:	Automatic/manual
Manual setting range:	PROG pattern; 10^{-n} (n: 2, 3, 4, 5, 6, 7, 8, 9, 10) PRBS pattern; 10^{-n} (n: 2, 3, 4, 5, 6, 7)
Automatic synchronization:	Yes. User selectable
Re-synchronization (manual):	Yes. User selectable

Error Detection

Mode	
Omitting/Inserting/Total:	Omitting error (0's error), inserting error (1's error), and total error
Overhead/Payload/Total:	Overhead error, payload error and total error (OPTION 71)
Specific/Other/Total:	Specific field error, not specific field error and total error

Measurement Mask

Mask route:	1 to 16 (can be set to any value in increment of 1/16 bit route)

Received Pattern

Frequency:	10 MHz to 3.6 GHz

Pseudo random (PRBS) pattern

Pattern length:	2^n - 1 (n: 7, 9, 10, 11, 15, 23, 31)

Number of stages and generating function:

Number of stages	Generating function	Standard
7	$X^7 + X^6 + 1$	ITU-T recommended V. 29
9	$X^9 + X^5 + 1$	ITU-T recommended V. 52
10	$X^{10} + X^7 + 1$	
11	$X^{11} + X^9 + 1$	ITU-T recommended O. 152
15	$X^{15} + X^{14} + 1$	ITU-T recommended O. 151 (1/2)
23	$X^{23} + X^{18} + 1$	ITU-T recommended O. 151 (1/2)
31	$X^{31} + X^{28} + 1$	

Mark ratio (variable):	1/2, 1/4, 1/8, 0/8, 1/2, 3/4, 7/8, 8/8
Mark ratio and number of bit shift:	1 bit

Programmable (PROG) pattern

Pattern length:	1 to 8,388,608 (2^{23}) bit

Pattern length and variable setting resolution [bit]:

Pattern length range	Setting resolution
1 to 262,144	1
262,146 to 524,288	2
524,292 to 1,048,576	4
1,048,584 to 2,097,152	8
2,097,168 to 4,194,304	16
4,194,336 to 8,388,608	32

Zero substitution (ZSUB) pattern

Pattern length:	2^n (n: 7, 9, 10, 11, 15)

Continuous zero bit length and setting resolution [bit]:

ZSUB Pattern length	Continuous zero bit length range	Setting resolution
2^7	7 to 127	1
2^9	9 to 511	1
2^{10}	10 to 1023	1
2^{11}	11 to 2047	1
2^{15}	15 to 32767	1

STM (SONET/SDH) pattern (OPTION 71)

Frame structure:	STM-4, STM-16
Number of frames:	STM-4; 1 to 107 frames STM-16; 1 to 26 frames
Payload types:	Can be selected from PROG pattern and PRBS pattern
Scrambling:	Can be provided
B1 byte:	Can be provided

Flexible (FLEX) pattern (OPTION 71)

Number of patterns:	PROG pattern; 127 types PRBS pattern; 1 type
Pattern length:	PROG pattern; 128 to 65,536 bits (setting resolution; 64 bits) PRBS pattern; 128 to 2,097,152 bits (setting resolution; 64 bits)
Number of combined patterns:	1 to 1024 pattern(s)
Pattern logic:	Can be logically inverted

Burst

Mode:	External (the burst input is available)

Trigger

Mode:	Can be selected form 1/16 clock, Pattern phase (fixed), Frame (OPTION 71) and Flexible (OPTION 71)
Flexible (OPTION 71):	The Low level or High level can be set for each pattern

AUX

Mode:	Can be selected from Data type and synchronized status
Data type:	The Low level is output for PROG pattern The High level is output for PRBS pattern

Clock Input

Frequency:	10 MHz to 3.6 GHz
Termination and coupling:	DC termination, AC coupling
Input amplitude:	0.3 to 2 Vp-p
Input waveform:	Rectangular wave or Sine wave (175 MHz to 3.6 GHz) Rectangular wave (10 to 175 MHz)
Duty ratio:	50 ± 5%
Clock delay:	±1 ns (setting resolution; 1 ps)
Input impedance:	50Ω (nominal)
Termination voltage:	To GND: 0 V ECL (to -2 V); -2.3 to -1.7 V setting resolution: 50 mV PECL (to +3 V); +2.7 to +3.3 V setting resolution: 50 mV LVPECL (to +1.3 V); +1 to +1.6 V setting resolution: 50 mV CML (to Vcc); 0 to 3.5 V setting resolution: 50 mV
Polarity:	Can be inverted
Connector:	SMA female

Data Input

Frequency:	10 MHz to 3.6 GHz
Mode:	NRZ
Termination and coupling:	DC termination, DC coupling
Input amplitude:	0.3 to 2 Vp-p
Threshold voltage:	To GND; -2.040 to +2.040 V setting resolution: 1 mV ECL (to -2 V); -1.850 to -0.750 V setting resolution: 1 mV PECL (to +3 V); 3.150 to +4.250 V setting resolution: 1 mV LVPECL (to +1.3 V); +1.450 to +2.550 V setting resolution: 1 mV CML (to Vcc); Vcc -1.1 to Vcc +0.1 V setting resolution: 1 mV (Vcc: termination voltage)
Termination voltage:	To GND: 0 V ECL (to -2 V); -2.3 to -1.7 V setting resolution: 50 mV PECL (to +3 V); +2.7 to +3.3 V setting resolution: 50 mV LVPECL (to +1.3 V); +1 to +1.6 V setting resolution: 50 mV CML (to Vcc); 0 to 3.5 V setting resolution: 50 mV
Input impedance:	50Ω (nominal)
Polarity:	Can be inverted
Connector:	SMA female

Burst (Trigger) Input

Input level:	0/-1 V
Input impedance:	50Ω (nominal) to 0V
Connector:	SMA female

Error Output

Output level:	0/-1 V
Load impedance:	50Ω to 0 V
Connector:	SMA female

Trigger Output

Output level:	0/-1 V
Load impedance:	50Ω to 0 V
Connector:	SMA female

General Descriptions

Operating environment range:	+5 to +40°C Relative humidity; 40 to 85% (without condensation)
Storage environment range:	-20 to +70°C Relative humidity; 30 to 85% (without condensation)
Power consumption:	90 VA or below
Mass:	6 kg (13.2 lbs.) or less

3.6 GHz Synthesizer Module (OPTION 13)

Clock Signal Source

Generated frequency range:	10 MHz to 3.6 GHz
Frequency setting resolution:	1 kHz
Frequency accuracy:	Within ±2 ppm
SSB phase noise:	-85 dBc/Hz or less (10 kHz offset)
External reference:	Yes. See below for specifications

Clock Output

Output amplitude:	1.2 ±0.6 Vp-p (175 MHz ≤f ≤3.6 GHz) 0.7 ±0.4 Vp-p (10 MHz ≤f <175 MHz)
Output waveform:	Sine wave (175 MHz ≤f ≤3.6 GHz) Square wave (10 MHz ≤f <175 MHz)
Load impedance:	50Ω
Connector:	SMA female

10 MHz Output (when outputting the internal reference signal)

Frequency:	10 MHz
Frequency accuracy:	Within ±2 ppm
Output amplitude:	0 dBm ±5 dB
Coupling:	AC
Connector:	SMA female

10 MHz Input (when inputting the external reference signal)

Frequency:	10 MHz
Input level:	0 dBm ±5 dB
Coupling:	AC
Connector:	SMA female

General Descriptions

Operating environment range:	+5 to +40°C Relative humidity; 40 to 85% (without condensation)
Storage environment range:	-20 to +70°C Relative humidity; 30 to 85% (without condensation)
Power consumption:	80 VA or below
Mass:	3.5 kg (7.7 lbs.) or less

Jitter Tolerance (OPTION70)

Jitter Generation

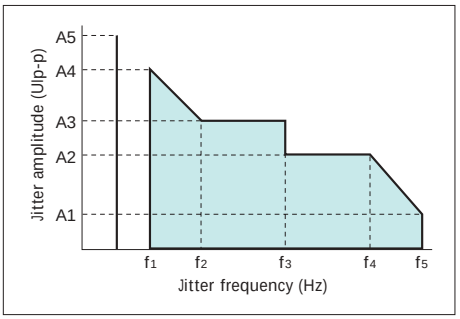
Clock frequency range: 10 to 3200 MHz
Band 1; 800 MHz ≤ clock frequency ≤3200 MHz
Band 2; 175 MHz ≤ clock frequency <800 MHz
Band 3; 10 MHz ≤ clock frequency <175 MHz

Clock frequency setting resolution: 1 kHz

Jitter frequency range: 10 Hz to 20 MHz (Band 1)
10 Hz to 5 MHz (Band 2)
10 Hz to 2 MHz (Band 3)

Jitter frequency setting resolution: 10 Hz

Jitter amplitude range: 0 to 800 UIp-p (Band 1, Band 2)
0 to 200 UIp-p (Band 3)



Band 1 (800 MHz ≤ clock frequency ≤3200 MHz)

Jitter frequency [Hz]	f_0	f_1	f_2 to f_3	f_3 to f_4	f_5
	10	20	200 to 5 k	5 to 300 k	20 M
Maximum Jitter amplitude [UIp-p]	A5	A4	A3	A2	A1
	800	500	50	20	0.3

Band 2 (175 MHz ≤ clock frequency ≤800 MHz)

Jitter frequency [Hz]	f_0	f_1	f_2 to f_3	f_3 to f_4	f_5
	10	20	200 to 5 k	5 to 125 k	5 M
Maximum Jitter amplitude [UIp-p]	A5	A4	A3	A2	A1
	800	500	50	20	0.5

Band 3 (10 MHz ≤ clock frequency ≤175 MHz)

Jitter frequency [Hz]	f_0	f_1	f_2 to f_3	f_3 to f_4	f_5
	10	20	200 to 5 k	5 to 200 k	2 M
Maximum Jitter amplitude [UIp-p]	A5	A4	A3	A2	A1
	200	120	12	5	0.5

Jitter amplitude accuracy: A reference standard; ITU-T O.172

Jitter amplitude setting resolution:

	Jitter amplitude setting range	Setting resolution
Band 1 Band 2	0 to 5 UIp-p 5 to 50 UIp-p 50 to 500 UIp-p 500 to 800 UIp-p	0.01 UIp-p 0.1 UIp-p 1 UIp-p 2 UIp-p
Band 3	0 to 1 UIp-p 1 to 10 UIp-p 10 to 100 UIp-p 100 to 200 UIp-p	0.01 UIp-p 0.1 UIp-p 1 UIp-p 2 UIp-p

Jitter Tolerance Measurement

Measurement mode: Can be selected from the following modes
Search mode; Jitter tolerance points are searched automatically
Sweep mode; Jitter tolerance at specified points are measured

Available option configurations table

Configurations	OPTION 10/11	OPTION 12	OPTION 13	OPTION 70	OPTION 71	OPTION 72
No. 1	NO	YES	NO	NO	NO	NO
No. 2	NO	YES	NO	NO	NO	YES
No. 3	YES	NO	YES	NO	NO	NO
No. 4	YES	NO	YES	NO	YES	NO
No. 5	YES	YES	YES	NO	NO	NO
No. 6	YES	YES	YES	YES	NO	NO
No. 7	YES	YES	YES	NO	YES	NO
No. 8	YES	YES	YES	NO	NO	YES
No. 9	YES	YES	YES	YES	YES	NO
No. 10	YES	YES	YES	YES	NO	YES
No. 11	YES	YES	YES	NO	YES	YES
No. 12	YES	YES	YES	YES	YES	YES

Please contact our office for other configurations.

Module options

OPTION 10: Pulse Pattern Generator (2 Vp-p output) module
OPTION 11: Pulse Pattern Generator (3 Vp-p output) module
OPTION 12: Error Detector module
OPTION 13: 3.6 GHz synthesizer module

Measurement function options

OPTION 70: Jitter Tolerance option
OPTION 71: Pattern option
OPTION 72: Error phase analysis option

Please be sure to read the product manual thoroughly before using the products.
Specifications may change without notification.

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